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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/717,966	11/21/2000	Martijn Johannes Lambertus Emons	PHN 17,746	9680

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
CAO, CHUN	
ART UNIT	**PAPER NUMBER**
2115	13

DATE MAILED: 03/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/717,966	EMONS, MARTIJN JOHANNES LAMBERTUS	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-10,12-14 and 16-19* is/are rejected.

7)☒ Claim(s) *3,11 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL REJECTION

1. Claims 1-19 are presented for examination. Claims 9-19 are newly added claims

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

3. Claims 1, 2, 4-10, 12-14, and 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Conary et al. (Conary), U.S. Patent No. 5,481,731.

The rejections of claims 1-2 and 4-8 are respectfully maintained and reproduced hereinbelow for applicant's convenience.

As per claim 1, Conary disclose a data processing system [computer system, fig. 1] which may be situated in a reduced-power mode, comprising a first data processing unit [a processor] that has access to a memory [a cache] belonging to the first data processing unit [col. 2, lines 11-14] and a second data processing unit [devices or main memory, col. 20, lines 1-4] that has access to the memory belonging to the first data processing unit [col. 2, lines 24-29; col. 19, line 60-col. 20, line 6; col. 21, lines 52-62];

characterized in that the first data processing unit is arranged for offering the second data processing unit access to the memory belonging to the first data processing unit in a reduced-power mode of the data processing system [col. 2, lines 24-29; col. 19, line 60-col. 20, line 6; col. 21, lines 52-62].

As per claim 2, Conary discloses that the first data processing unit is arranged for offering the second data processing unit access to the memory belonging to the first data processing unit in a period of time in which the reduced-power mode of the data

processing system implies a reduced-power mode of the first data processing unit [col. 2, lines 24-29; col. 19, line 60-col. 20, line 6; col. 21, lines 52-62].

As per claim 4, Conary discloses that the memory belonging to the first data processing unit forms part of the first data processing unit [fig. 2].

As per claim 5, Conary discloses that the memory belonging to the first data processing unit is a cache memory [fig. 2; col. 4, lines 61-62].

As per claim 6, Conary discloses that the first data processing unit is a microprocessor [fig. 2; col. 4, lines 61-62].

As per claim 7, Conary discloses a video controller [a display device, col. 4, line 22. Since the computer system comprises a display device, it would have been obvious to one of ordinary skill in the art to include a video controller in order to control video display in the display device].

As per claim 8, Conary discloses a data processing unit having access to a memory belonging to the data processing unit which data processing unit may be situated in a reduced-power mode, characterized in that the data processing unit is arranged for offering access in the reduced-power mode to the memory belonging to the data processing unit [col. 2, lines 24-29; col. 19, line 60-col. 20, line 6; col. 21, lines 52-62].

As per claim 9, Conary discloses a mechanism that allow the first data processing unit to offer a second data processing unit access to the memory belonging to the first data processing unit in the reduced-power mode [col. 2, lines 24-29; col. 19, line 60-col. 20, line 6; col. 21, lines 52-62].

As per claim 10, Conary discloses the second memory unit can be accessed by system components other than the first data processing unit in the reduced-power mode [col. 19, line 60-col. 20, line 6].

As per claim 12, Conary discloses that the memory belonging to the first data processing unit is a cache memory [fig. 2; col. 4, lines 61-62].

10. As per claim 13, Conary disclose a data processing system [computer system, fig. 1] which may be situated in a reduced-power mode having a first data processing unit [a processor] that has access to a first memory [a cache] associated with the first data processing unit [col. 2, lines 11-14] and a second data processing unit [other devices or main memory, col. 20, lines 1-4] that has access to the first memory [col. 2, lines 24-29; col. 19, line 60-col. 20, line 6; col. 21, lines 52-62] comprising;

a second memory associated with the second data processing unit [col. 19, line 60-col. 20, line 6]; and

a mechanism that allow the first data processing unit to offer the second data processing unit access to the first memory belonging to the first data processing unit in a reduced-power mode of the data processing system [col. 2, lines 24-29; col. 19, line 60-col. 20, line 6; col. 20, lines 30-32; col. 21, lines 52-62].

As per claim 14, Conary discloses the second memory unit can be accessed by system components other than the first data processing unit in the reduced-power mode [col. 19, line 60-col. 20, line 6].

As per claim 16, Conary discloses that the memory belonging to the first data processing unit forms part of the first data processing unit [fig. 2].

As per claim 17, Conary discloses that the memory belonging to the first data processing unit is a cache memory [fig. 2; col. 4, lines 61-62].

As per claim 18, Conary discloses that the first data processing unit is a microprocessor [fig. 2; col. 4, lines 61-62].

As per claim 19, Conary discloses a video controller [a display device 121, col. 4, line 22. Since the computer system comprises a display device, it would have been obvious to one of ordinary skill in the computer art to include a video controller in order to control video display for the display device].

4. Claim 8 is rejected under 35 U.S.C. 102(b) as being anticipated by Carmean et al. (Carmean), U.S. Patent No. 5,669,003.

The rejection of claim 8 is respectfully maintained and reproduced hereinbelow for applicant's convenience.

As per claim 8, Carmean discloses a data processing unit having access to a memory belonging to the data processing unit which data processing unit may be situated in a reduced-power mode, characterized in that the data processing unit is arranged for offering access in the reduced-power mode to the memory belonging to the data processing unit [col. 6, lines 11-22; col. 7, lines 58-63].

5. Applicant's arguments filed on 1/10/2004 have been fully considered but are not persuasive.

6. In the remarks, applicant argued in substance that [1] **Conary** does not disclose any mechanism for the processor to offer access to a memory that belongs to the

processor. [2] In claim 8, **Carmean** does not disclose a processor offering accessing to a memory resource that is belonged to the processor.

7. As to [1], the examiner traverses applicant's argument. In the claim language of claim 1, "any mechanism for the processor to offer access to a memory that belongs to the processor ". In the other words, a memory belongs to the processor can be accessed by other data processing unit [According to the specification of the present application, page 4, lines 14-18]. Conary discloses a mechanism for the processor offer access to a memory (an internal cache) that belongs to the processor [col. 2, lines 24-29; col. 19, line 60-col. 20, line 6; col. 21, lines 52-62]. In summary, Conary discloses an internal cache belonging to the processor can be accessed (writing data to the internal cache for maintaining data coherency) by a main memory or other devices [col. 2, lines 24-29; col. 19, line 60-col. 20, line 6; col. 21, lines 52-62; col. 22, lines 1-17].

As to [2], Carmean discloses a processor offering accessing to a memory resource that is belonged to the processor [col. 6, lines 11-22, 33-35; col. 7, lines 58-63. emphasis added "The local caches of the processors...If any data is cached in one of the processor and another processor attempts to access the data...].

Allowable Subject Matter

8. Claims 3, 11 and 15 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao at (703) 308-6106. The examiner can normally be reached on Monday-Friday from 7:30 am - 4:00 pm. If attempts to reach the examiner by phone are unsuccessful, the examiner's supervisor Thomas Lee can

be reached at (703) 305-9717. The fax number for this Art Unit is following: Official (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 306-5631.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chun Cao

Mar. 15, 2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100